

This listing of claims will replace all prior versions, and listings, of claims in the application:

**The Status of the Claims**

1. (Currently Cancelled)
2. (Currently Amended) A method as defined in claim [[1]] 3,  
wherein the spacers are formed by depositing and etching a SiN layer.
3. (Currently Amended) A method of fabricating a memory cell comprising:  
forming spacers to isolate and protect a gate area including a floating gate and a control gate;  
forming a gap filling layer over a substrate including the gate area and the spacers; and  
depositing an insulating layer over the gate area and the gap filling layer, A method as defined in claim 1, wherein the gap filling layer is formed by depositing undoped polysilicon or amorphous silicon over the gate area and the spacers, and by performing an anisotropic etching of the deposited undoped polysilicon or amorphous silicon.
4. (Currently Amended) A method as defined in claim [[1]] 3,  
wherein the insulating layer is formed of TEOS (tetra ethyl ortho silicate) or BPSG (borophosphorsilicate glass).

5. (Currently Cancelled).

6. (Currently Amended) A memory cell structure as defined in claim [[5]] 7, wherein the spacers are formed of SiN.

7. (Currently Amended) A memory cell structure comprising:  
a plurality of gate areas, the gate areas including a gate oxide, a floating gate, an insulating layer, and a control gate;  
spacers on sidewalls of the gate areas;  
a gap filling layer formed in gaps between the spacers of the gate areas; and  
an insulating layer deposited over the gate areas and the gap filling layer, as defined in claim 5, wherein the gap filling layer is formed of undoped polysilicon or amorphous silicon.

8. (Original) A memory cell structure as defined in claim 7, wherein the gap filling layer is formed by an anisotropic etching.

**Please add the following new claims:**

9. (New) A method of fabricating a memory cell comprising:  
forming spacers to isolate and protect a gate area including a floating gate and a control gate;  
forming a non-etch resistant gap filling layer over a substrate including the gate area and the spacers; and

depositing an insulating layer over the gate area and the gap filling layer.

10. (New) A memory cell structure comprising:  
a plurality of gate areas, the gate areas including a gate oxide, a floating gate, an insulating layer, and a control gate;  
spacers on sidewalls of the gate areas;  
a non-etch resistant gap filling layer formed in gaps between the spacers of the gate areas; and  
an insulating layer deposited over the gate areas and the gap filling layer.